IN THE SPECIFICATION:

Page 4, lines 2 - 11:

The invention will be better understood by reference to the following more detailed description and accompanying drawings in which

FIG. 1 is a high-level block diagram of a conventional per-pin tester architecture;

FIG. 2 is a high-level block diagram of a conventional shared resource tester architecture;

FIG. 3 is a high-level block diagram of a hybrid tester architecture according to one form of the present invention; and

FIG. 4 is a flowchart illustrating a method of testing a plurality of semiconductor devices with the hybrid tester architecture of Figure 3.